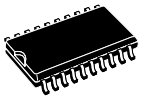
74LVX273

LOW VOLTAGE CMOS OCTAL D-TYPE FLIP-FLOP WITH CLEAR (5V TOLERANT INPUTS)

- HIGH SPEED:
  f_{MAX} = 150 MHz (TYP.) at V_{CC} = 3.3V
- 5V TOLERANT INPUTS
- POWER-DOWN PROTECTION ON INPUTS
- INPUT VOLTAGE LEVEL:
  V_{IL} = 0.8V, V_{IH} = 2V at V_{CC} =3V
- LOW POWER DISSIPATION:
  I_{CC} = 4 µA (MAX.) at T_A=25°C
- LOW NOISE:
  V_{OLP} = 0.3V (TYP.) at V_{CC} =3.3V
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN) at V_{CC} =3V
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 273
- IMPROVED LATCH-UP IMMUNITY



SOP

TSSOP

Table 1: Order Codes

PACKAGE	T & R
SOP	74LVX273MTR
TSSOP	74LVX273TTR

DESCRIPTION

The 74LVX273 is a low voltage CMOS OCTAL D-TYPE FLIP-FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

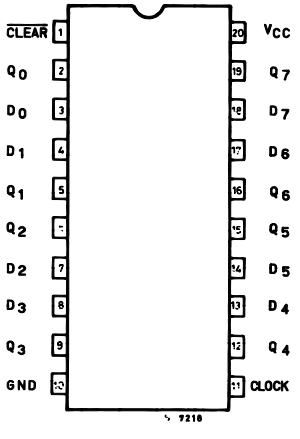
When the CLEAR input is held low, the Q outputs are held low independently of the other inputs.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V. It combines high speed performance with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols



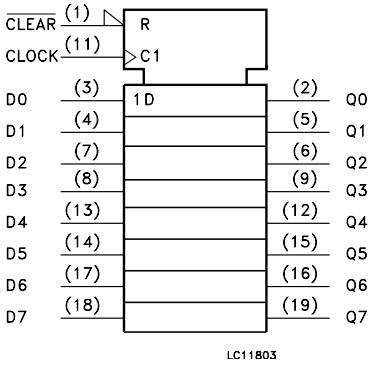


Figure 2: Input Equivalent Circuit

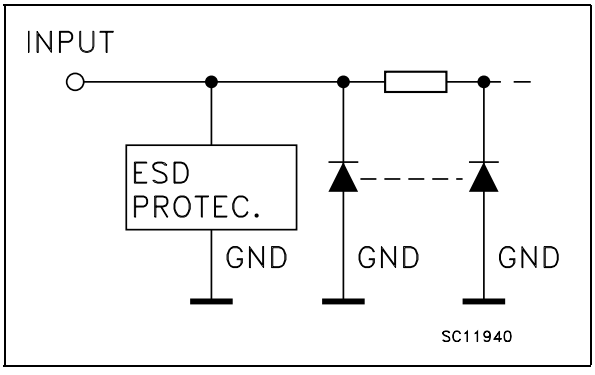


Table 2: Pin Description

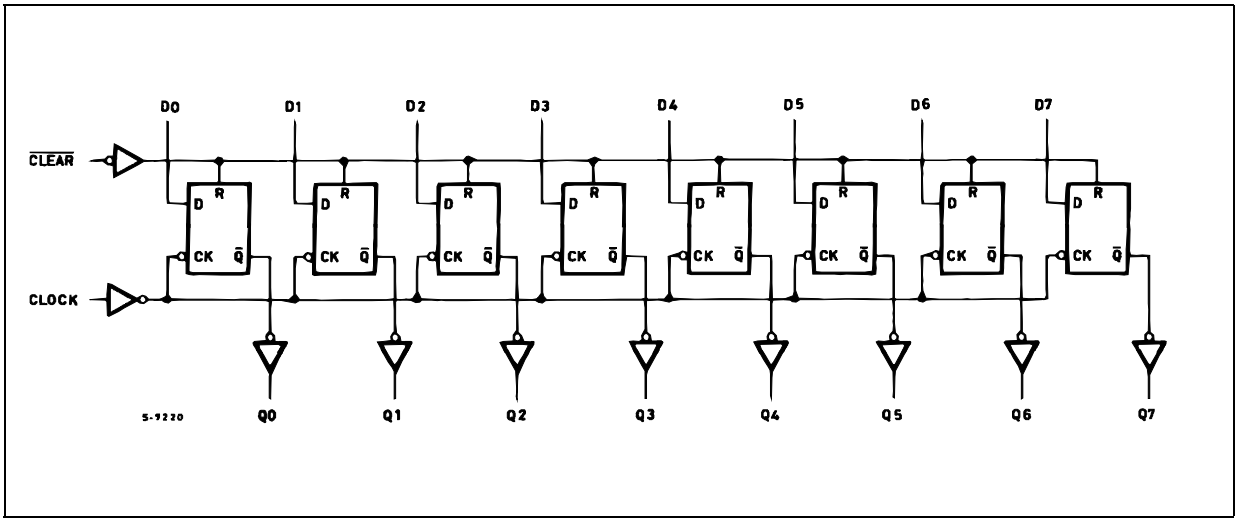
PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Asynchronous Master Reset (Active LOW)
2, 5, 6, 9, 12, 15, 16,19	Q0 to Q7	Flip-Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW-to-HIGH Edge Triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	B	Q	
L	X	X	L	CLEAR
H	L	↑	L	
H	H	↑	H	
H	X	↓	Q_n	NO CHANGE

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) (V_{CC} = 3V)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2.0V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		2.9		
		3.0	I_O=-4 mA	2.58			2.48		2.4		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44		0.55	
I_I	Input Leakage Current	3.6	V_I = 5V or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND			4		40		40	µA

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.3	0.8					V
V_{OLV}				-0.8	-0.3						
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics (Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q	2.7	15			9.0	16.9	1.0	20.5	1.0	22.0	ns
		2.7	50			11.5	20.4	1.0	24.0	1.0	25.5	
		3.3(*)	15			7.1	11.0	1.0	13.0	1.0	14.5	
		3.3(*)	50			9.6	14.5	1.0	16.5	1.0	18.0	
t_{PHL}	Propagation Delay Time $\overline{CLEAR}$ to Q	3.3(*)	15			9.3	17.6	1.0	20.5	1.0	22.0	ns
		3.3(*)	50			11.8	21.1	1.0	24.0	1.0	25.5	
		5.0(**)	15			7.3	11.5	1.0	13.5	1.0	15.5	
		5.0(**)	50			9.8	15.0	1.0	17.0	1.0	18.0	
$t_{W(L)}$	$\overline{CLEAR}$ pulse Width, HIGH	2.7	50				5.0		6.0		6.0	ns
		3.3(*)					5.0		5.0		5.0	
t_W	CLOCK pulse Width, HIGH	2.7	50				5.5		6.5		6.5	ns
		3.3(*)					5.0		5.0		5.0	
t_S	Setup Time Q to CLOCK HIGH or LOW	2.7	50				5.5		6.5		6.5	ns
		3.3(*)					4.5		4.5		4.5	
t_h	Hold Time Q to CLOCK HIGH or LOW	2.7	50				1.0		1.0		1.0	ns
		3.3(*)					1.0		1.0		1.0	
t_{REM}	Recovery Time $\overline{CLEAR}$ to Q	2.7	50				2.5		2.5		2.5	ns
		3.3(*)					2.0		2.0		2.0	
f_{MAX}	Maximum Clock Frequency	2.7	15		55	110		55		50		MHz
		2.7	50		45	60		40		35		
		3.3(*)	15		95	150		80		75		
		3.3(*)	50		60	90		55		50		
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1,2)	2.7	50			0.5	1.0		1.5		1.5	ns
		3.3(*)	50			0.5	1.0		1.5		1.5	

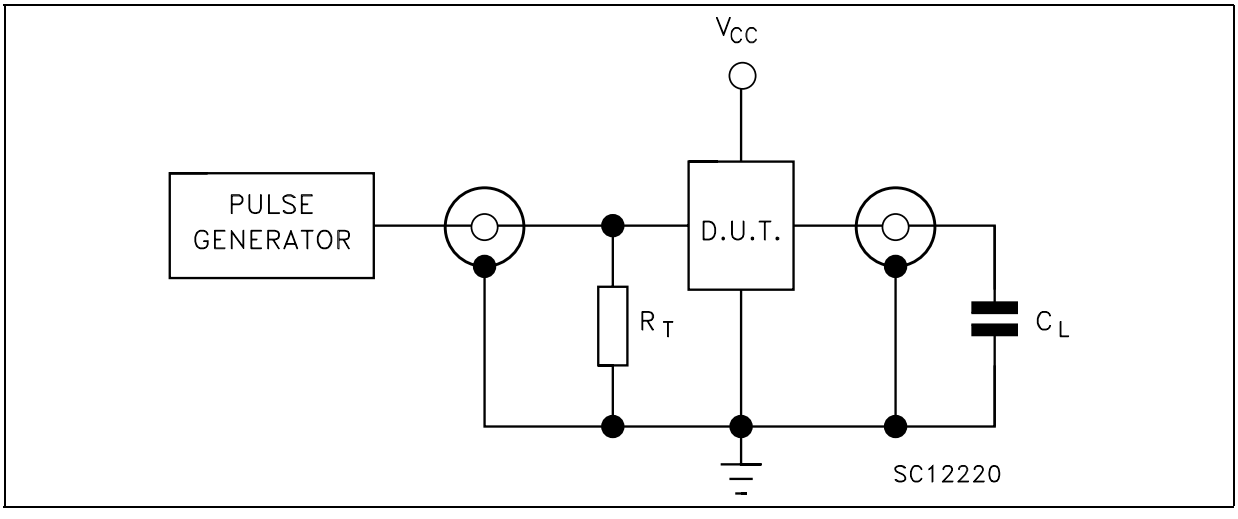
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW
2) Parameter guaranteed by design
(*) Voltage range is 3.3V ± 0.3V

Table 4: CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz		40						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without ad. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

Figure 5: Test Circuit



C_L =15/50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 6: Waveform - Propagation Delays (f=1MHz; 50% duty cycle)

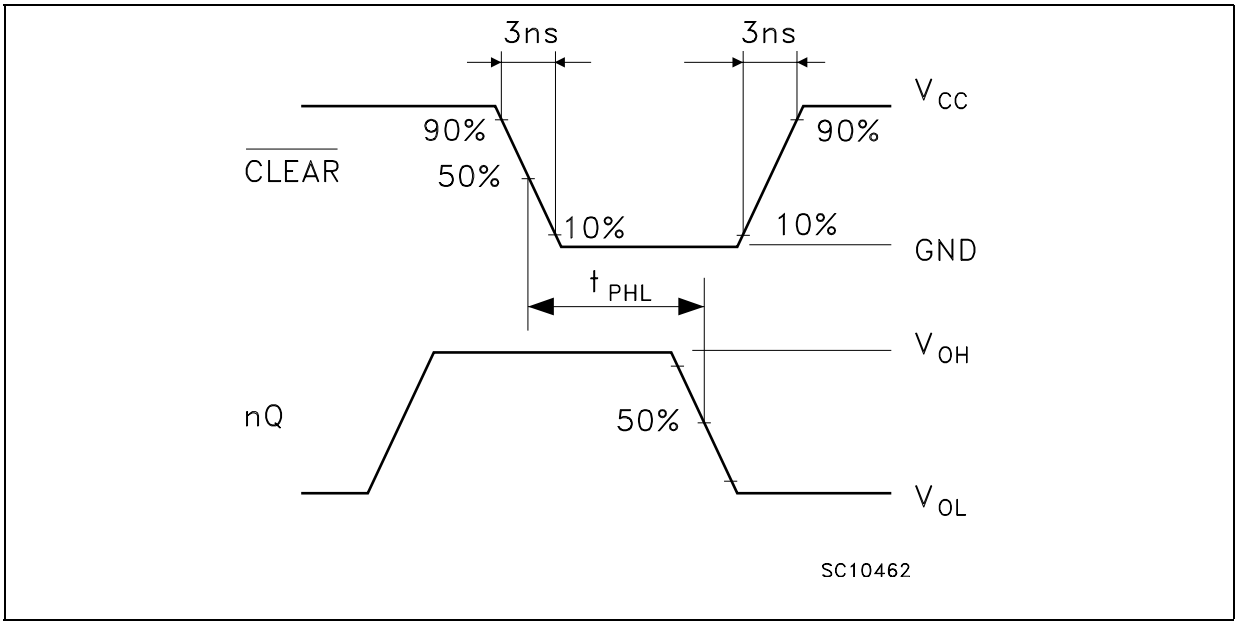


Figure 7: Waveform - Propagation Delays, Setup And Hold Times (f=1MHz; 50% duty cycle)

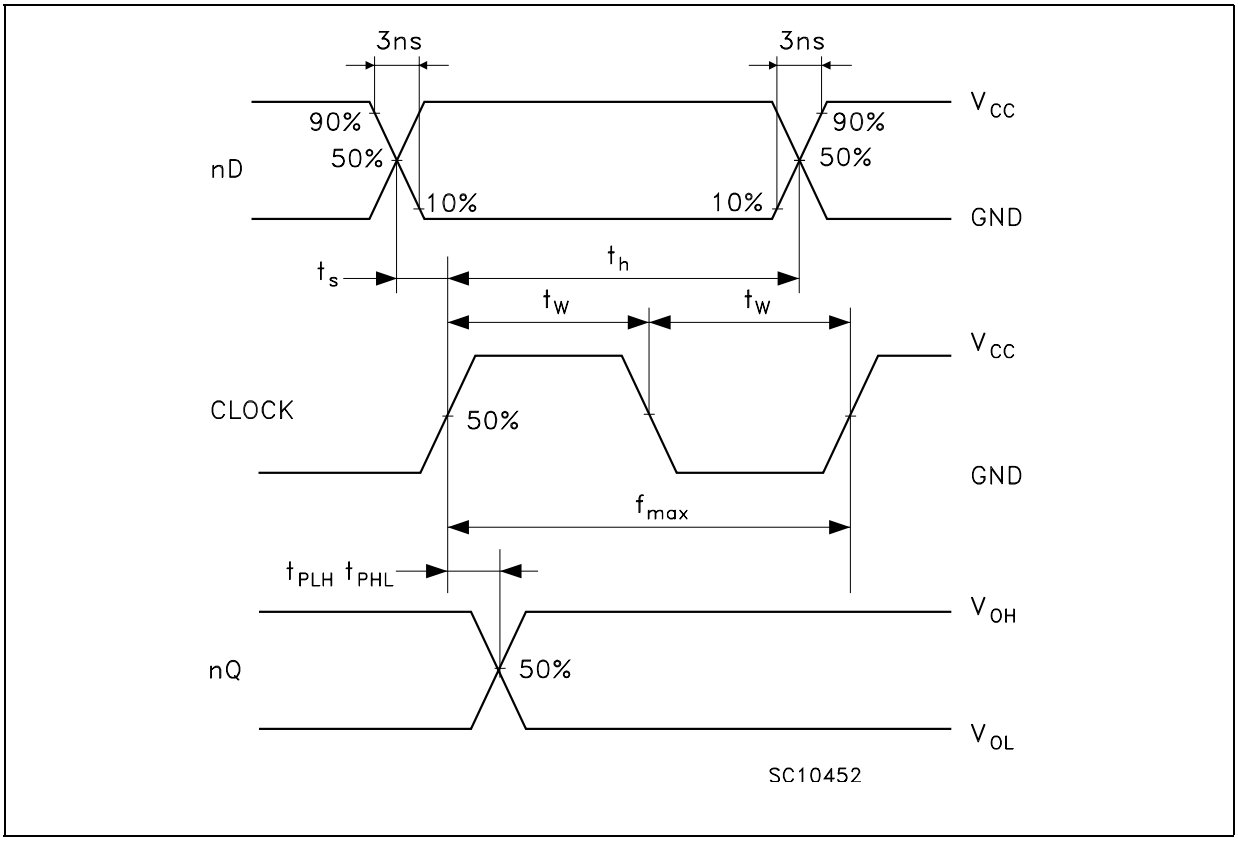
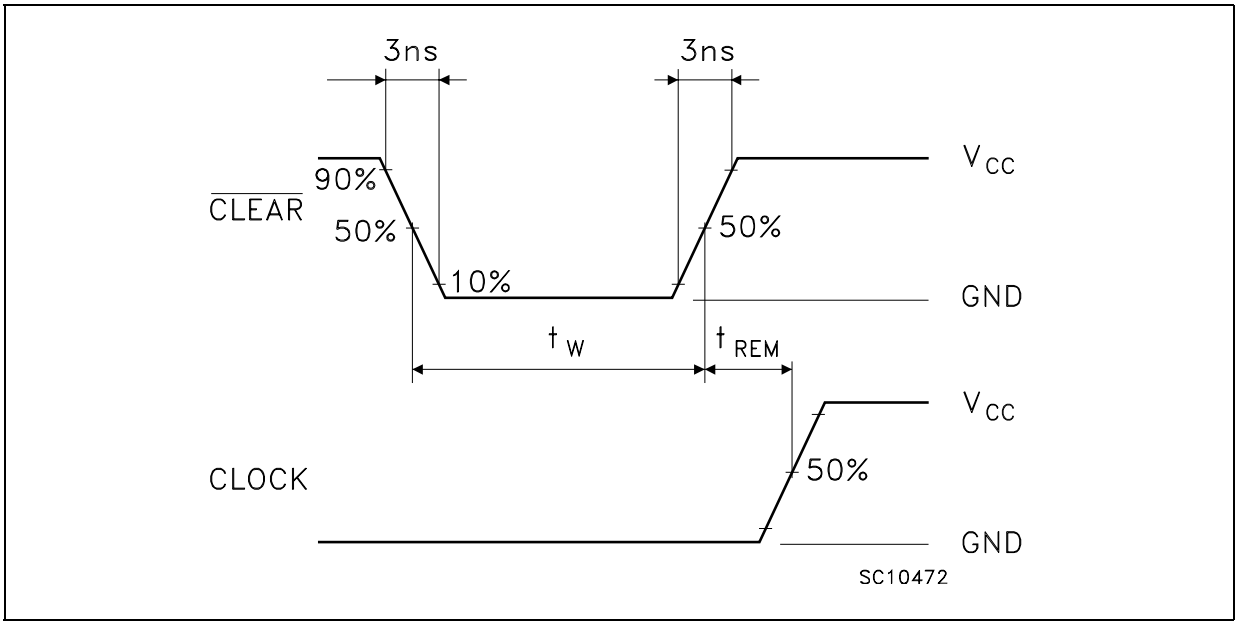
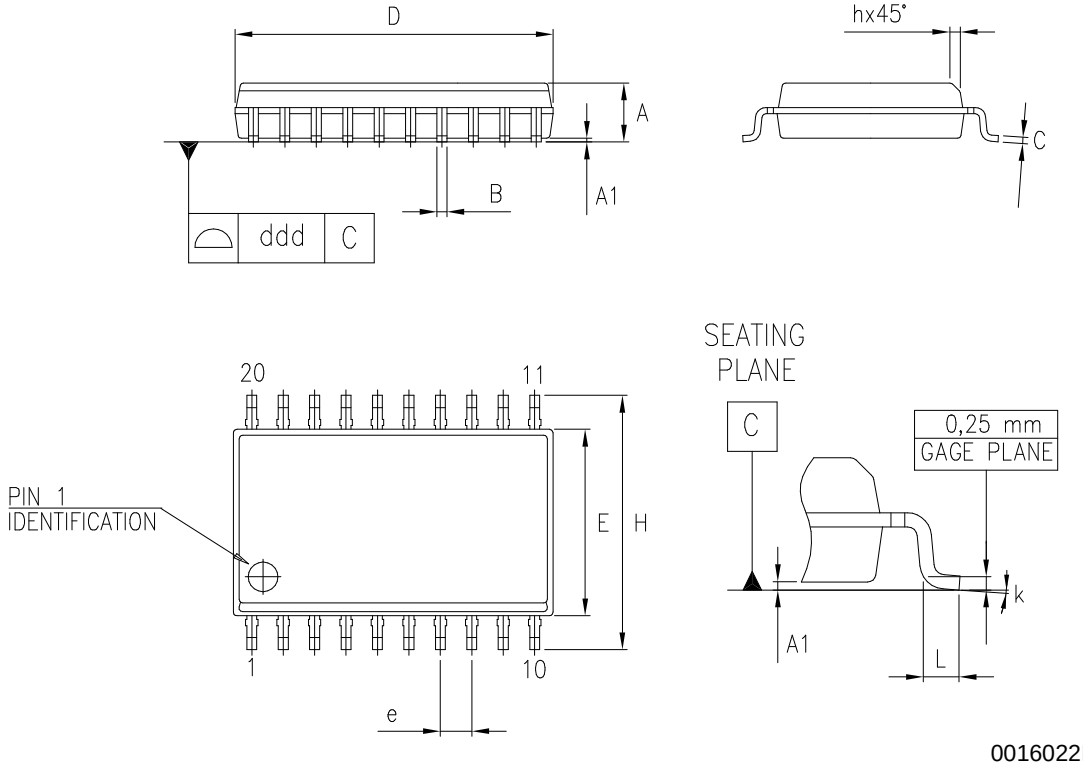


Figure 8: Waveform - Recovery Time (f=1MHz; 50% duty cycle)



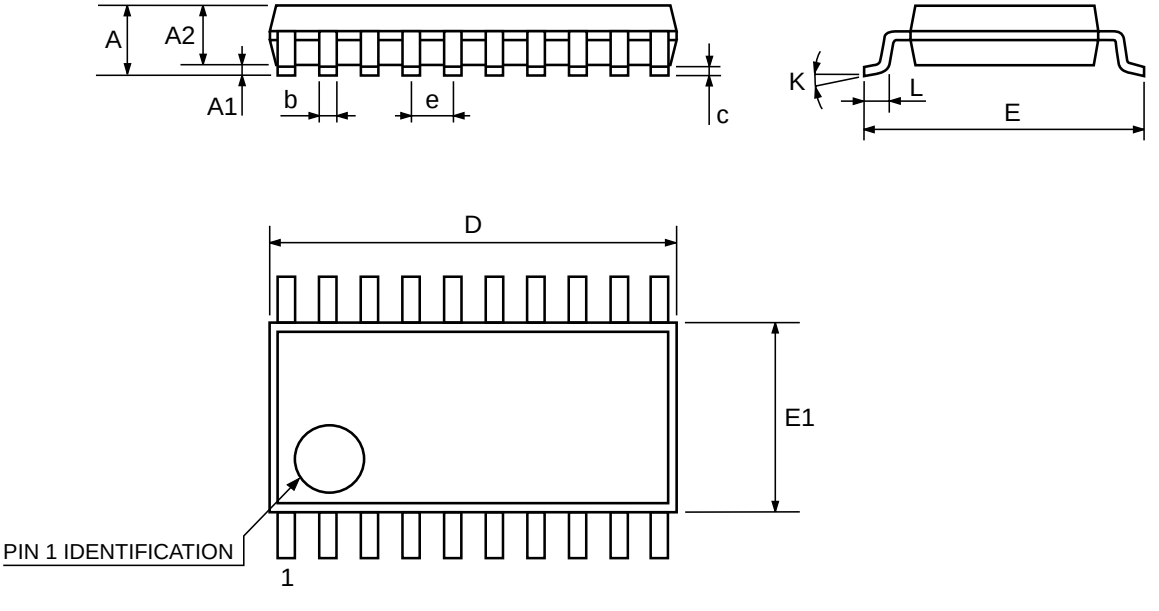
SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



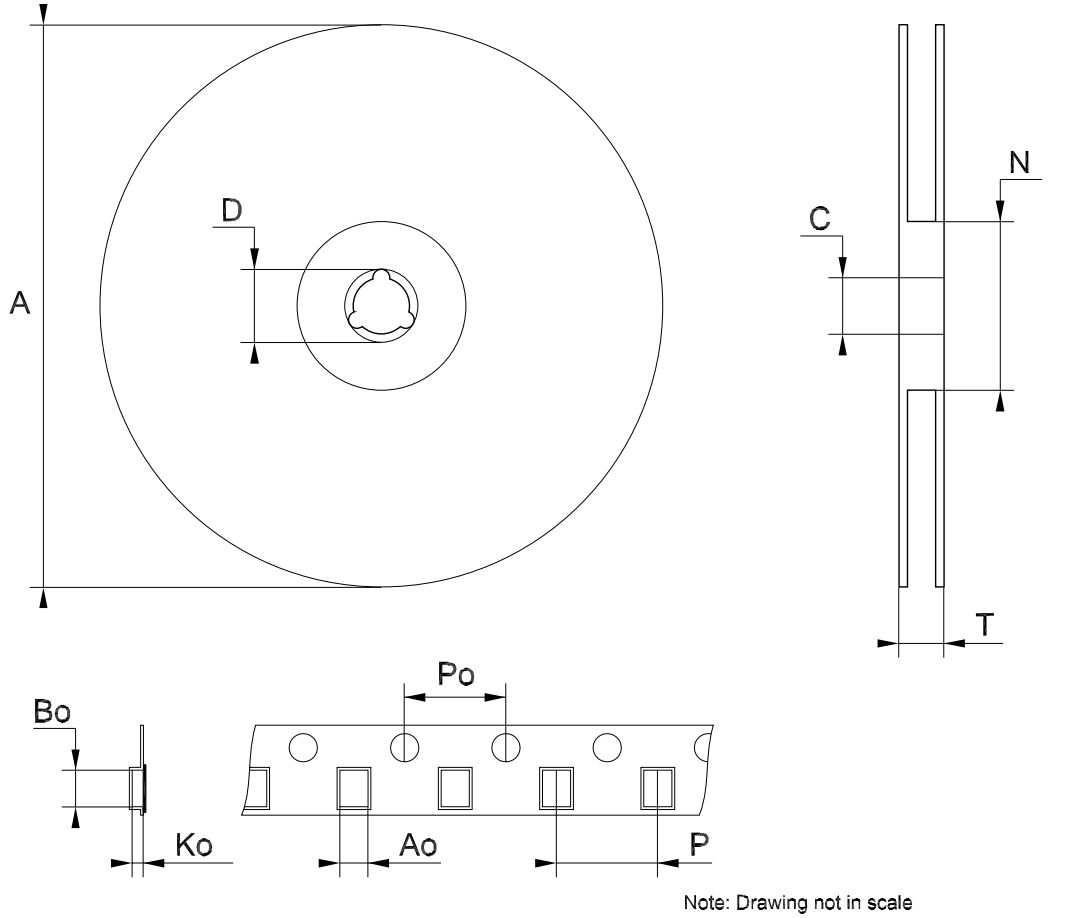
TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-20 MECHANICAL DATA

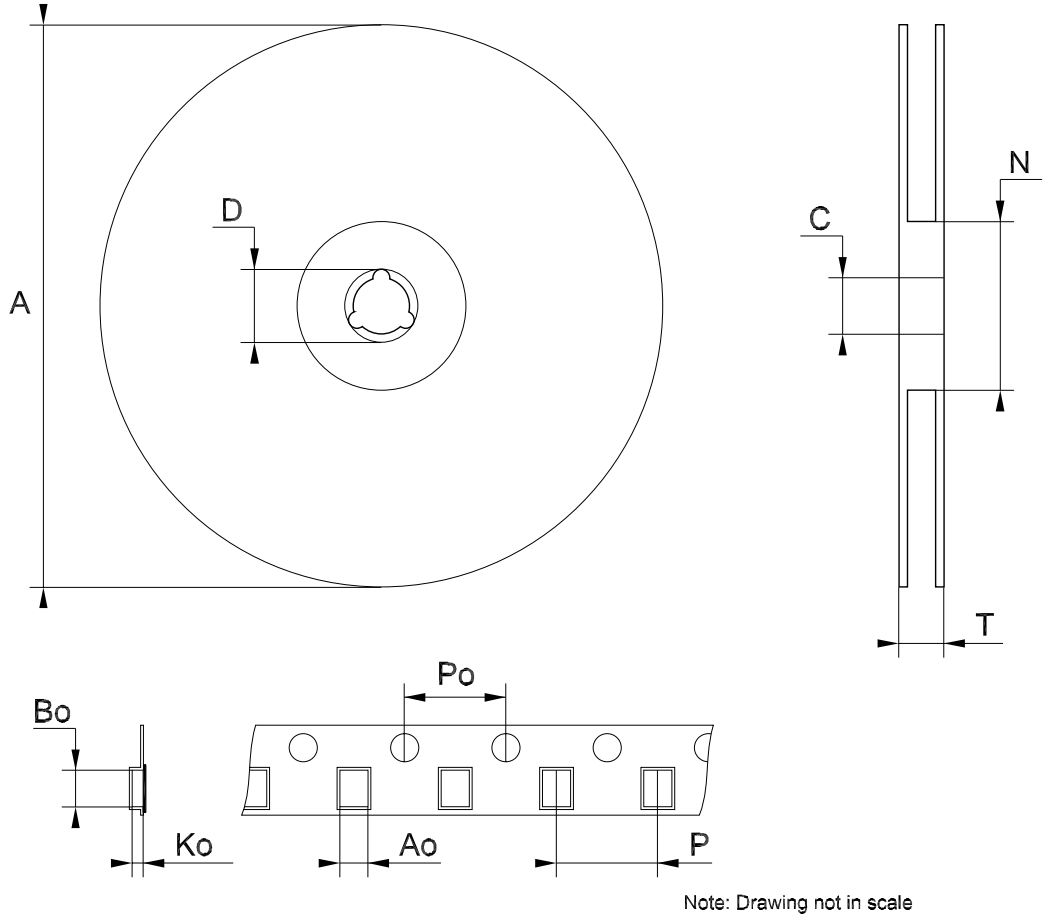
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

Table 9: Revision History

Date	Revision	Description of Changes
27-Aug-2004	3	Ordering Codes Revision - pag. 1.

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